Power µElectronics Directions for the Future

by

John W. Klein, Karla B. Clark, Greg Carr, Mark L. Underwood, and Leon J. Alkalaj
Jet Propulsion Laboratory
Pasadena, CA 91109

Abstract

This paper will discuss the results of the µElectronics roadmaps developed for the New Millennium Program. The roadmaps will place into perspective the future directions power µElectronics will need to take in order to be compatible with 3-D Avionics packages for future spacecraft architectures. The paper will also discuss baseline avionic system architectures for the New Millennium Flight Projects.

New Millennium Program

In early 1995, NASA Headquarters charged JPL to develop a program that would "enable 21st-Century missions through the identification, development, and flight validation of key technologies". To identify the highest priority technologies for development, government, industry, and academia were asked to participate in Integrated Product Development Teams (IPDTs): µElectronics, Autonomy, Telecom, Mechanical and Multifunctional Systems, and MicroElectromechanical Systems. Each of these IPDTs have developed roadmaps stating which technologies for the 21st-Century are required and their development schedule.

To validate these technologies, a number of deep space and Earth observing missions are planned. These missions were selected based upon the readiness of various technologies at the time of project start. The first three deep space missions have been selected and approved while the Earth observing mission set is under development. Deep Space 1 is due to launch in January 1998, Deep Space 2 in 99, and Deep Space 3 in 01. Interim dates are expected for the Earth observing missions.

Deep Space 1 will be a asteroid and comet flyby utilizing Solar Electric Propulsion (SEP). New technologies demonstrated on this mission will be advanced µElectronics, SEP, advanced solar arrays, autonomous navigation, and advanced rechargeable batteries. The solar arrays will be delivered to JPL by BMDO as a validation of the Scarlet Array. This will be a true team effort between government agencies to fly and validate new

[1] "New Millennium Program Plan", JPL D 12623, April 14, 1995, p1.

technologies. BMDO will deliver the Scarlet Array, a new multi-bandgap solar array capable of delivering more power than typical single junction cells. Air Force Phillips Lab will participate in the validation of advanced µElectronics. Their previous commitment to funding advanced technology has given µElectronics a headstart in validating advanced technologies for the 21st Century.

Deep Space 2 will be a MicroLander/Penetrator that will be a piggyback experiment on the Mars '98 mission. It will perform some fundamental science and will validate many advanced electronics/telecom systems, as well as advanced instruments.

Deep Space 3 is scheduled to be an interferometry mission. There will be three spacecraft flying in formation forming the interferometer. Advanced technologies will include autonomy, advanced structures, advanced telecom.

µElectronics IPDT

The µElectronics IPDT participants were selected through an evaluated process **where interested members** submitted a ten page proposal on their technology. The selected members are:

- Leon Alkalai - CoLead, JPL
- Danny Dalton - CoLead, GSFC
- Capt. Ron Marx - Air Force Phillips Laboratory
- Bob Delean - Loral Federal **Systems**
- Darby Terry - TRW
- Dr. John Samson - Honeywell
- Dr. Robert Kalman - Optivision
- Nick Teneketges - Space Computer Corporation
- Gerhard Franz - Lockheed Martin Corporation
- - Sandia National Laboratory
- - MIT Lincoln Labs.

This membership has been participated in the development of a µElectronics Roadmap. This roadmap has been broken into the following areas:

I Processors
  A General Purpose Processors
  B µControllers
  C Digital Signal Processing
II Storage
III Input/Output
IV Power µElectronics
V Low Power Synthesis and Architectures
VI Packaging

Processors

Due to the responses received through the first call and the limited funds available for the total program only General Purpose Processors was chosen for detail roadmapping in this first phase, Figure 1 shows a graphical representation of the roadmap.

Notice that the processing speed continues to increase while the mass continues to fall. It appears that the technology may be reaching a plateau in terms of mass but the processing speed is expected to continue to grow.

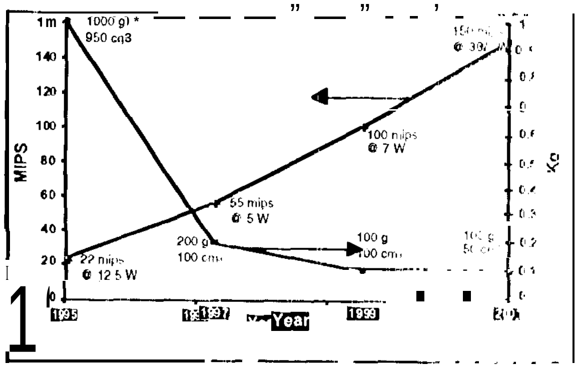

Figure 1. General Purpose Processor Roadmap

By and large the entire IPDT felt it important to develop radiation hardened processors so that the core of the avionics was "bullet-proof'. While many of the NASA missions do not require radiation hardened processors, the knowledge that such are available and that no single event upset can destroy a critical sequence is assuring. Secondly, it was felt that well established operating systems and design environments are the wave of the future. Specialized operating systems that change from mission to mission arid development tools that change just as quickly add cost, complexity, and schedule to projects for the future. With the advent of 12 - 18 month projects, this overhead can not be accepted.

Storage

Non volatile memory has been the focus of the IPDT to date. With the advent of competitive flash technologies along with other more robust radiation hardened technologies, the IPDT felt it advisable to be looking at non-volatile Solid State Recorders as their first option. The storage roadmap is shown in Figure 2.

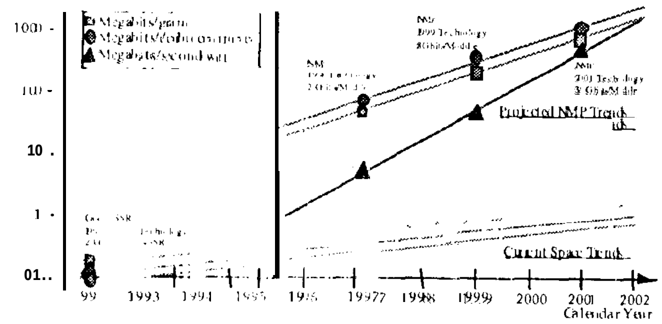

Figure 2. Storage Roadmap

1 he dramatic changes in the storage arena make it very difficult to predict what technologies will be available and when. The Figure shows that memory densities will continue to escalate, It is anticipated that solid state recorders (SSRs) in the Gbyte range will be available in 2000 timeframe. This coupled with the*' large advances in non-volatile memories means that reduced power and archiving earl be accomplished on board. Recent discussions have talked about the use of Flash to replace E E PROM in some cases. The IPDT is looking into this possibility.

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The requirements for Input/Output varies widely over the Deep Space and Earth Observing mission set. Due to the limited communication link speed to Earth, Deep Space missions normally do not require high bandwidth I/O systems except within the computer and possibly its links to local memory and the SSR. Other than this, most of the communications can be accomplished over lower bandwidth systems in the 1 to 10 Mbit/sec range. Deep Space missions also have a very hard requirement on mass and power. Due to the limited amount of power available for Deep Space missions, the amount of power available for this function is extremely limited. The standard implementation of 1553 using up to 2 Watts per node is extremely intensive. A much lower standby power and smaller volume implementation meets the needs of Deep Space missions.

Earth Observing missions are quite the opposite. Due to the large amounts of data taken **and directly** shipped to Earth, large bandwidths are required. Fiber Optic Data Busses of up to 600 Mbits/sec are required in the 21st-Century. Also, due to the larger nature of their solar arrays and the capability to extract more energy being closer to the sun allows more flexibility in the implementation. Thus, the higher power implementations of FODB are well within the trade space for Earth Observing missions.

To meet this broad spectrum an all encompassing roadmap was developed. Figure 3 shows that roadmap.

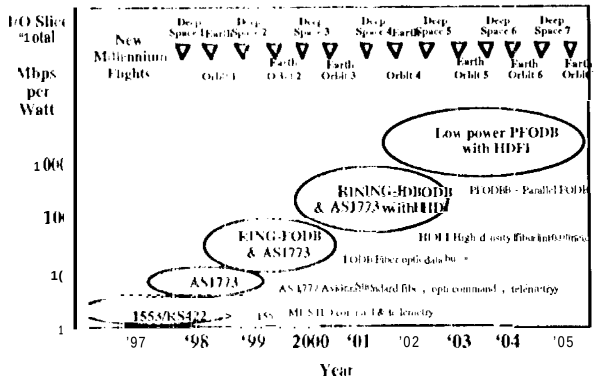


Figure 3. Input/Output Roadmap

While the capability of the I/O link continues to increase, it is also important to note that the IPDT recognized the need to reduce its power requirements at the same time. The standard 1553 and its fiber optic derivative 1773 are extremely power intensive. For small spacecraft where point to point I/O is required this can be an overhead that is unacceptable. Thus, this area will couple closely with the low power synthesis area to develop new 1773 systems that are low in power, mass, and volume.

Packaging

The prime goal of all the µElectronics area is to shrink the physical size of the various subelements to such a stage that compact 3D packaging implementations can be used. To accomplish this, each subelement (processors, local memory, SSR, and input/Oulput) will be packaged in 2D Multi Chip Modules (MCMs)/ Theses MCMs will then be packaged in a 3D configuration. Figure 4 shows a concept for such an implementation.

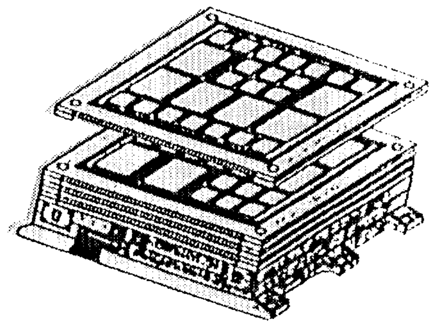


Figure 4. 3D MCM Stack

The goal of this element will be to produce as much functionality as possible in the smallest space. Early on flights will use a mechanical means to achieve this package. Later flights Will incorporate advanced schemes to achieve even greater densities.

Power µElectronics

Unlike the digital field which has seen dramatic increases in functionality accompanied with similar reductions in size, the analog field has not kept pace. One of the prime goals of the New Millennium Program is to kick start this situation so that analog, analog and digital, and digital circuits all reside within the same packaging constraints. While the above packaging scheme may accommodate the entire avionics digital electronics in a ICI x 10 x 8 cm package, the power µElectronics associated with the rest of the avionics package will be an order of magnitude larger if current packaging techniques arc used. Thus, to be compatible with the above packaging schemes the advances shown in Figure 5 must be achieved.

It is quite apparent from studying the roadmap that power µElectronics has a long and difficult road ahead. It must achieve performance measurements at least two orders of magnitude better than current State of Practice (SOP). Only in this way can the analog technologies of the future be packaged in such a way as to be compatible with 3D stacking techniques.

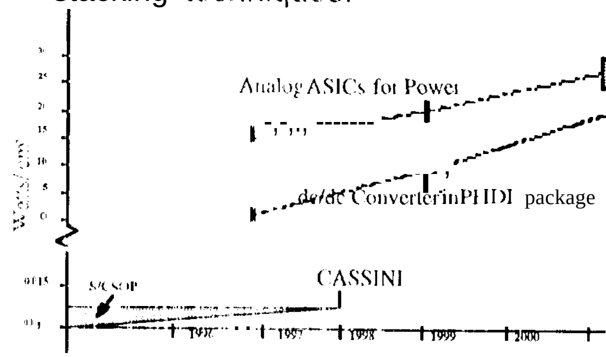


Figure 5. Power µElectronics Roadmap

There are two technologies of fundamental interest to the power µElectronics activity; mixed signal ASICs and power high density interconnect (PHDI) techniques. The mixed signal ASIC development involves the integration of analog and digital circuits into the same package. While hybrid circuits are an early form of this technology, recent advances allow for much greater integration. This means that the digital circuitry to control an analog function can now be integrated with the actuation function, In addition, the package is so small that it can be easily integrated at the point of use. This concept, while not implemented on

Flight 1 of New Millennium, is a goal for power μ Electronics.

This roadmap of all others requires patience and long term commitment. So little R&D funding has been spent in this arena compared to the digital field that great strides will not be made overnight. New Millennium will take a long term, reasonable risk approach. The first flight will incorporate mixed signal ASICs and de/de converters implemented in PHDI. Figure 6 shows what a typical PHDI implementation for a de/de converter might look like. Notice that the transformer still dominates the landscape for converters. While a lot of effort has been spent over the past years in ultra high frequency conversion to reduce the size of magnetics, large technical issues remain unresolved. I-bus, innovative hybrid and other packaging schemes have come to the forefront. F light 1 will incorporate these concepts on VME cards for ease of integration. Later flights will integrate the power μElectronics right onto the stack. In this way the most compact implementation can be achieved.

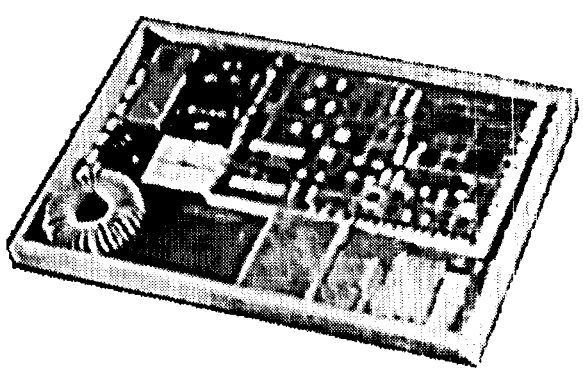


Figure 6. Prototype **Layout** of dc/dc converter in PHDI

Flight 1 Avionics Architecture

With the above set of roadmaps, it is the job of the F light 1 Team and the IPDT to develop an avionics architecture that will verify the technologies along the roadmaps. For Flight 1 the architecture of Figure 7 has been recommended. It is very similar to the architectures of past flights but will utilize new technologies from the roadrnaps.

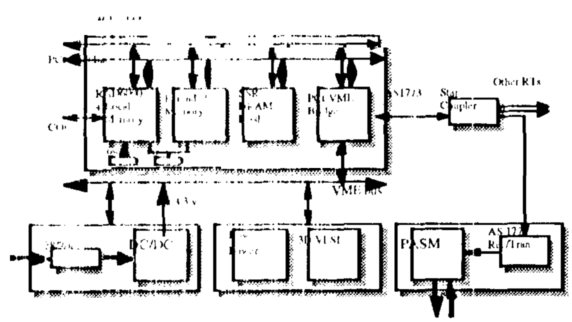


Figure 7. Flight 1 Avionics Architecture

The processor will be an advanced radiation hardened 5 0 MIP processor with up to 160 Mbytes of local memory. It will utilize the VXworks real time operating system and be compatible with a PC I data bus. 1 his "subsystem" will be packaged in 2 MCMs that can be utilized in a 3D structure.

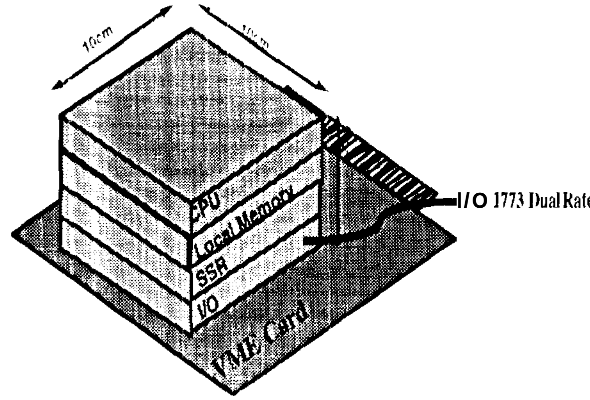
The SSR will contain 2 Gbits of storage; 1Gbit of DRAM and 1 Gbit of Flash. Due to the differences in read anti write access of the two types of storage, special access logic and programming will be employed to take! full advantage of the available memory. This "subsystem" will also be packaged in an MCM.

The I/O capabilities will be handled by various mixed signal ASIC designs. The **1/0** "subsystem" must allow the avionics system to talk with the VME backplane as well as the 1773 **data bus.** Thus, the I/O "subsystem" will have a PCI to VME conversion and interface and a PCI to 1773 conversion and interface.

The Power Switching and Activation Module (PASM) is the backbone of the power distribution network, It is a set of 16 switches built with one of the advanced technologies into one small package. The PASM will control turnon 'of all loads, limit in rush current, trip on overcurrent, and recycle when tripped. It will also give status and telemetry on each switch when poled.

Flight 1 Implementation

Due to the complexity of adding so many new technologies within a very short period of time, it has been decided to break up the stack into high bandwidth users and low bandwidth users. The high bandwidth users will utilize the PCI bus as it means of communication. Thus the Processor/Local Memory slice(s), the SSR slice, and the I/O slice will be packaged together into one core block. To facilitate integration into the spacecraft, the block will be placed onto a standard 6U VME card. Additional analysis will need to be performed to determine how best to support and transfer heat from the stack, Figure 8 shows a graphic of this implementation



f" igure 8. Flight 1 "Core"Avionics Implementation

The analog sections will be separated and integrated separately to facilitate more develop and checkout time. Figure 9 demonstrates these implementations.

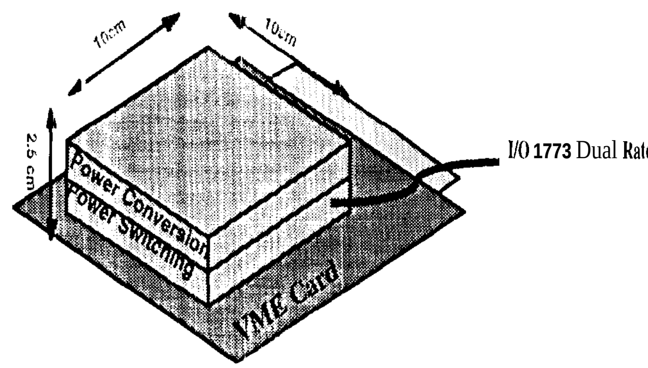


Figure 9. PASM and de/de Converter Implementation

Notice that each of this implementation is compatible with the '(core" stack shown in Figure 8. Thus, for flight 3 or other opportunity, the power µElectronics will be packaged with the core avionics structure yielding a very compact, highly functional, integrated package.

Conclusions

Power Electronics of the future will need to packaged into smaller sizes that fit with the packaging concepts for 3D multi-chip modules, These point of load converters and power distribution/control systems will allow for the implementation of remote power switching, micro-spacecraft implementations, and unique micro-instrument applications.

Unfortunately, this will riot happen on its own. Continued long term support is needed in the field to continue to push the technology pipeline. Failure to do so will only widen the current "size gap" between the functionality/size figure of merit for digital systems and analog or mixed mode systems. The Department of Defense and NASA are working to continue development of this pipeline.

Acknowledgements